

HARDWARE SOFTWARE CO-DESIGN USING SYSTEM VERILOG

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Abstract

Hardware/Software Co-design is a cooperative design of hardware and software components. One of the goals of Co-design is to shorten the time-to-market while reducing the design effort and costs of the designed products. The flexibility of software allows late design changes and simplified debugging opportunities. Furthermore, the possibility of reusing software by porting it to other processors reduces the time-to-market and the design effort. However, the designer always use hardware when processors are not able to meet the required performance. This trade-off between hardware and software illustrates the optimization aspect of the Co-design problem. This paper presents framework for Research work to analyse effectiveness of System Verilog for system level modelling and Co-design. It further discusses how system Verilog can be used for modelling software components as well as hardware components of the system. One method is also proposed to carry out the Co-simulation and Codesign. Paper also discussed the expected results from the proposed work.

Keywords : Codesign, System Verilog , Modelsim 10.1c.Verilog

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